REMARKS

The application has been carefully reviewed in light of the Office Action dated March 12, 2003. Claims 3, 7-9, 17, 21-23, 31, 35-37 and 48 have been cancelled without prejudice. Claims 1, 15, 24, 29, 38 and 41 have been amended. Claims 49-51 are newly added. Claims 1, 2, 4-6, 10-16, 18-20, 24-30, 32-34, 38-47 and 49-51 are now pending in this case.

Figures 1 and 2 stand objected to as not being designated "Prior Art." Applicants respectfully submit herewith a Proposed Drawing Correction with marked-up version of Figures 1 and 2. Favorable consideration is respectfully requested.

Claim 36 stands objected to due to a typographical error. Claim 36 has been cancelled and, therefore, this objection is no longer applicable.

Claims 1-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of Nelson et al. (U.S. Patent No. 5,258,660). Applicants respectfully traverse the rejection and request reconsideration.

Claims 3, 7-9, 17, 21-23, 31, 35-37 and 48 have been cancelled and, therefore, the rejection is no longer applicable to those claims.

Claims 1, 15 and 29 each recite a data output apparatus comprising a plurality of adjustable delay circuits, where "each adjustable delay circuit contains a programmable circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse for programming." [Emphasis added].

As acknowledged in the Office Action, neither AAPA nor Nelson expressly discloses these limitations. Nonetheless, the OA states that it would have been obvious to combine the two references and to replace the multiplexer with fuse elements. Applicants submit this is not proper grounds for a rejection under § 103.

According to MPEP § 2143, three basic criteria must be met in order to establish a prima facie case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art (at the time of the invention), to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference, or references when combined, must teach or suggest all the claim limitations.

Taking the third requirement first, even as acknowledged in the Office Action, neither reference, taken alone or in combination teaches or suggests all of the limitations of amended claims 1, 15 and 29. Further, neither reference provides any suggestion or motivation to be combined with the other, much less that a fuse element should be included in the programming circuit.

At least for those reasons mentioned above, a prima facie case of obviousness has not been made in the Office Action and claims 1, 15 and 29 are allowable over AAPA and Nelson.

Claim 41 recites a method of providing data output signals comprising "programming each respective adjustable delay by modifying a conductive state of at least one of a fuse element and an anti-fuse element to select a delay rate." At least for those reasons mentioned above in connection with claims 1, 15 and 29, claim 41 is also allowable over AAPA and Nelson.

Claims 2, 4-6, 10-14, 16, 18-20, 24-28, 30, 32-34 and 38-47 depend from claims 1, 15 and 29 and are allowable at least for those reasons mentioned above and also because the combination of AAPA and Nelson fails to teach or suggest their respective inventive combinations.

Claims 49-51 are respectively essentially identical to claims 1, 15 and 29, except that claims 49-51 recite at least one "anti-fuse element" rather than a fuse element. At

least for the reasons mentioned above in connection with claims 1, 15 and 29, claims 49-51 are allowable over AAPA and Nelson.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version with Markings to Show Changes Made

1. (Amended) A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective [first] delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element for programming.

15. (Amended) A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective

clock signal, and wherein each programming circuit contains at least one fuse element for programming.

24. (Amended) A processor based system as in claim [21] 20 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

29. (Amended) A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element for programming.

38. (Amended) A memory device as in claim [35] 34 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

41. (Amended) A method of providing data output signals comprising:

receiving a plurality of data output signals at respective output circuits; and

operating said output circuits in response to respective applied clock signals to make said data output signals available at the output of said output circuits;

providing a first clock signal; [and]

generating each said respective applied clock signal from said first clock signal, each said respective applied clock signals having a respective adjustable delay relative to said first clock signal; and

programming each respective adjustable delay by modifying a conductive state of at least one of a fuse element and an anti-fuse element to select a delay rate.